

REMARKS

Claims 21-40 are now pending in this application. Claims 27-28, and 35-37 have been amended. New claims 38-40 have been added. Support for the new claims can be found in the specification. No new matter has been added.

Claims 21-26 stand rejected under 35 U.S.C. § 112 first paragraph. Claims 27-31 and 33-36 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kao et al. (U.S. Patent Number 5,492,847). Claims 32 and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kao et al. in view of Gilgen et al. (U.S. Patent Number 5,134,085). Claims 21-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilgen et al. in view of Stolmeijer et al. (U.S. Patent Number 5,384,279). Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilgen et al. in view of Stolmeijer et al. and Icel et al. (U.S. Patent Number 5,248,624). Claims 25 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilgen et al. in view of Stolmeijer et al. and Kao et al.

Formalities

Claims 21-26 stand rejected under 35 U.S.C. § 112 first paragraph. Specifically, the office action states that “it is not clear how a single mask can be used to accomplish depositing a field implant, depositing a well implant and depositing an enhancement implant.” (Office action mailed January 5, 2001, page 3, paragraph number 5). That it is possible to use one mask for these three implants is explained in the specification, for example on page 9, line 37 to page 10, line 10, and shown in the Figures, for example Figures 2A and 2B.

It is understood by one of skill in the art that there are at least two examples of when implants are of no importance to a device structure, and may left off cross-section diagrams. One is when the doping of an implant is much less than that of a surrounding diffusion or implant, the other is when an implant is removed in distance from the area of interest.

The well implant defines the well, as shown in the specification, for example at page 10, lines 11-12. It would be understood by one skilled in the art that the enhancement implant covers the well, but is “outnumbered” or blocked everywhere except in the channel, where it is shown, for example in Figure 2A and 2B. The field implant also covers the same area, but is implanted with a higher energy level, as shown in the specification, for example on page 10, lines 6-7. This enables the field to be implanted below the isolation region, as shown, for example, in

Figures 2A and 2B. It would be understood by one skilled in the art that in the area between the isolation regions, the field implant is significantly deeper than the source and drain regions, and does not effect device operation.

Claim 27

Claims 27 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Kao et al. But Kao et al. do not teach each and every limitation of this claim. For example, claim 27, as amended, recites “wherein the first pocket implant is approximately in contact with the second pocket implant.” Kao et al. do not teach this feature.

In Kao et al. the implants do not approximately contact each other. Specifically, Figure 2(g) in Kao et al. shows implant areas 232 below the source and drain region portions 262. The channel edges of the implant areas are shown to be coincident with the source and drain regions. In the device of Figure 2(g), the source drain regions cannot approximately contact each other; if they do, the device will not perform properly. Thus, Kao et al. teach away from manufacturing a structure wherein the first pocket implant is approximately in contact with the second pocket implant. If such a structure is made following the teaching of Kao et al., the source and drain regions would be too close for proper device operation. Accordingly, claim 27 should be allowable for at least these reasons.

Claim 35

Claims 35 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Kao et al. But Kao et al. do not teach each and every limitation of this claim. For example, claim 35, as amended, recites “causing the first pocket implant to merge with the second pocket implant.” Again, Kao et al. show in Figure 2(g) a device with channel edges of implants 232 coincident with channel edges of the source drain region portions 262. If the pockets were to merge, the source drain regions would merge, and the device would be nonfunctional as a MOS enhancement mode device. Thus, Kao et al. teach away from having a device wherein the first pocket implant merges with the second pocket implant. Accordingly, claim 35 should be allowable for at least these reasons.

Claim 21

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilgen et al. in view of Stolmeijer et al. But Gilgen et al. and Stolmeijer et al., when combined, do not show or suggest each and every feature of this claim. For example, claim 21 recites “wherein the

depositing a field implant, depositing a well implant, and depositing an enhancement implant are done using a single mask.” The combination of Gilgen et al. and Stolmeijer et al. do not show or suggest this feature.

Specifically, Stolmeijer et al. is cited in the office action as showing the use of one mask for three implants. (Office action mailed January 5, 2001). But Stolmeijer et al. does not show or suggest this. Rather, Stolmeijer et al. in Figure 1 shows the use of mask 8 for two implants. Specifically, implants 10 and 11 are made using mask 8. See for example, see Stolmeijer et al., column 2, lines 39-42, which refers to the two implants as n-well and anti-punch-through implantation. See also Stolmeijer et al. column 6, lines 57-64. Accordingly, the combination of Gilgen et al. and Stolmeijer et al. show the use of one mask for two implants, and does not show the depositing a field implant, depositing a well implant, and depositing an enhancement implant using a single mask as is required by the claim. Accordingly, claim 21 should be allowable for at least these reasons.

Other claims

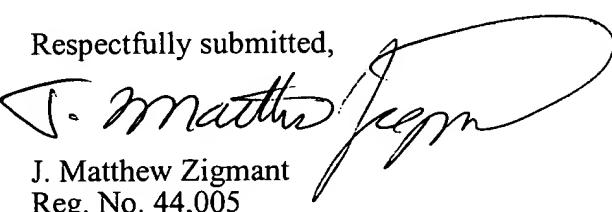
Claims 22-26 depend from claim 21, and should be allowed for the same reason as claim 21, and for the additional limitations they recite. Claims 28-34 depend from claim 27, and should be allowed for the same reason as claim 27, and for the additional limitations they recite. Claims 36-37 depend from claim 35, and should be allowed for the same reason as claim 35, and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



J. Matthew Zigmant  
Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, 8<sup>th</sup> Floor  
San Francisco, California 94111-3834  
Tel: (415) 576-0200  
Fax: (415) 576-0300  
JMZ  
PA 3153666 v1

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

1           27. (Amended) A method of fabricating a transistor in an integrated circuit  
2 device comprising:  
3           providing a semiconductor substrate;  
4           forming a gate oxide on the semiconductor substrate;  
5           forming a gate on the gate oxide;  
6           implanting a first pocket implant into the semiconductor substrate from a first side of  
7 the gate; and  
8           implanting a second pocket implant into the semiconductor substrate from a second  
9 side of the gate, wherein the first pocket implant is approximately in contact with the second pocket  
10 implant [; and  
11           **diffusing the first pocket implant and the second pocket implant laterally in the**  
12 **semiconductor substrate**].

1           28. (Amended) The method of claim 27 [wherein the first pocket implant is  
2 in contact with the second pocket implant] further comprising diffusing the first pocket implant  
3 and the second pocket implant laterally in the semiconductor substrate.

1           35. (Amended) A method of fabricating a transistor in an integrated circuit  
2 device comprising:  
3           providing a semiconductor substrate;  
4           forming a gate oxide on the semiconductor substrate;  
5           forming a gate on the gate oxide;  
6           implanting a first pocket implant and a second pocket implant into the semiconductor  
7 substrate using the gate as a mask; and  
8           diffusing the first and second pocket implants laterally causing the first pocket  
9 implant to merge with the second pocket implant [to increase a reverse short channel effect of the  
10 transistor].

1           36. (Amended) The method of claim 35 wherein the diffusing [causes the first  
2    **pocket implant to merge with the second pocket implant]** increases a reverse short channel effect  
3    of the transistor.

1           37. (Amended) The method of claim 35 further comprising implanting an  
2    enhancement implant in the semiconductor [implant] substrate.